

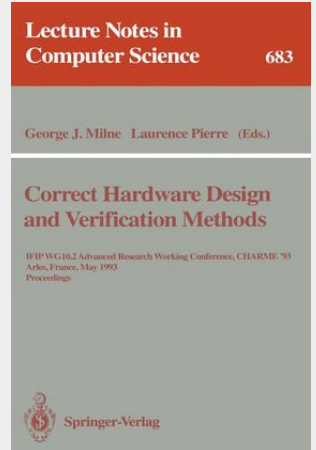
Pierre / Milne

Correct Hardware Design and Verification Methods

IFIP WG 10.2 Advanced Research Working Conference, CHARME'93, Arles, France, May 24-26, 1993. Proceedings

These proceedings contain the papers presented at the Advanced Research Working Conference on Correct Hardware Design Methodologies, held in Arles, France, in May 1993, and organized by the ESPRIT Working Group 6018 CHARME-2 and the Universit de Provence, Marseille, in cooperation with IFIP Working Group 10.2. Formal verification is emerging as a plausible alternative to exhaustive simulation for establishing correct digital hardware designs. The validation of functional and timing behavior is a major bottleneck in current VLSI design systems, slowing the arrival of products in the marketplace with its associated increase in cost. From being a predominantly academic area of study until a few years ago, formal design and verification techniques are now beginning to migrate into industrial use. As we are now witnessing an increase in activity in this area in both academia and industry, the aim of this working conference was to bring together researchers and users from both communities.

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53,49 €

49,99 € (zzgl. MwSt.)

Lieferfrist: bis zu 10 Tage

Artikelnummer: 9783540567783

Medium: Buch

ISBN: 978-3-540-56778-3

Verlag: Springer Berlin Heidelberg

Erscheinungstermin: 12.05.1993

Sprache(n): Englisch

Auflage: 1993

Serie: Lecture Notes in Computer Science

Produktform: Kartoniert

Gewicht: 435 g

Seiten: 275

Format (B x H): 155 x 235 mm

